

PLD (Programmable Logic Device)

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Prepared : Vandikas I.

Boolean expression

2 - bit full Adder with Carry In

$$S = A' * B' * C + A' * B * C' + A * B * C + A * B' * C'$$

A' = A inverted

Electronics Workbench

The screenshot displays the Multisim software interface. The main window is titled "Circuit1" and shows a grid for circuit design. A "Component Browser" dialog box is open, listing various 7400-series components. The "7408N" component is selected in the list. The dialog box provides detailed information for the selected component, including its symbol (ANSI), database name, component family, component name, footprint, and function. It also displays model data and manufacturer information.

Component Browser

Component Name List:

- 7400N
- 7402N
- 7403N
- 7404N
- 7405N
- 7406N
- 7407N
- 7408N**
- 7409N
- 74107N
- 74109N
- 7410N
- 74116N
- 74125N
- 74126N
- 7412N
- 74132N
- 74145N
- 74147N
- 74148N
- 7414N
- 74150N
- 74151N

Symbol (ANSI):

Database Name: Multisim Master

Component Family: 74STD

Component Name: 7408N

Footprint: N014

Function: QUAD 2-INPUT AND

Model Data:

.MODEL 7408 d_and (rise_delay = 27n fall_delay = 19n)

Manufacturer Name: Texas Instruments

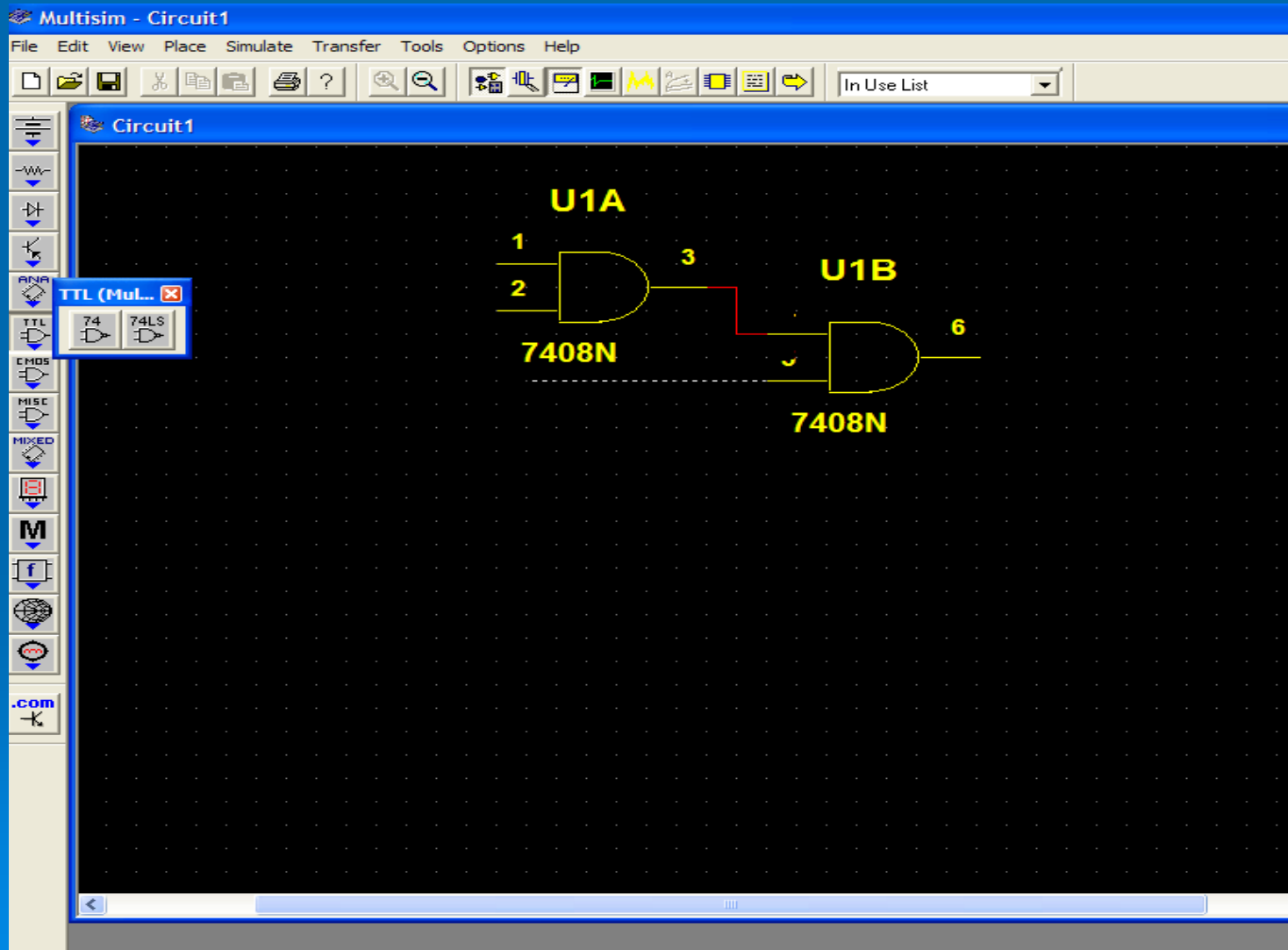
Model Level - ID: L0-7408

Operations:

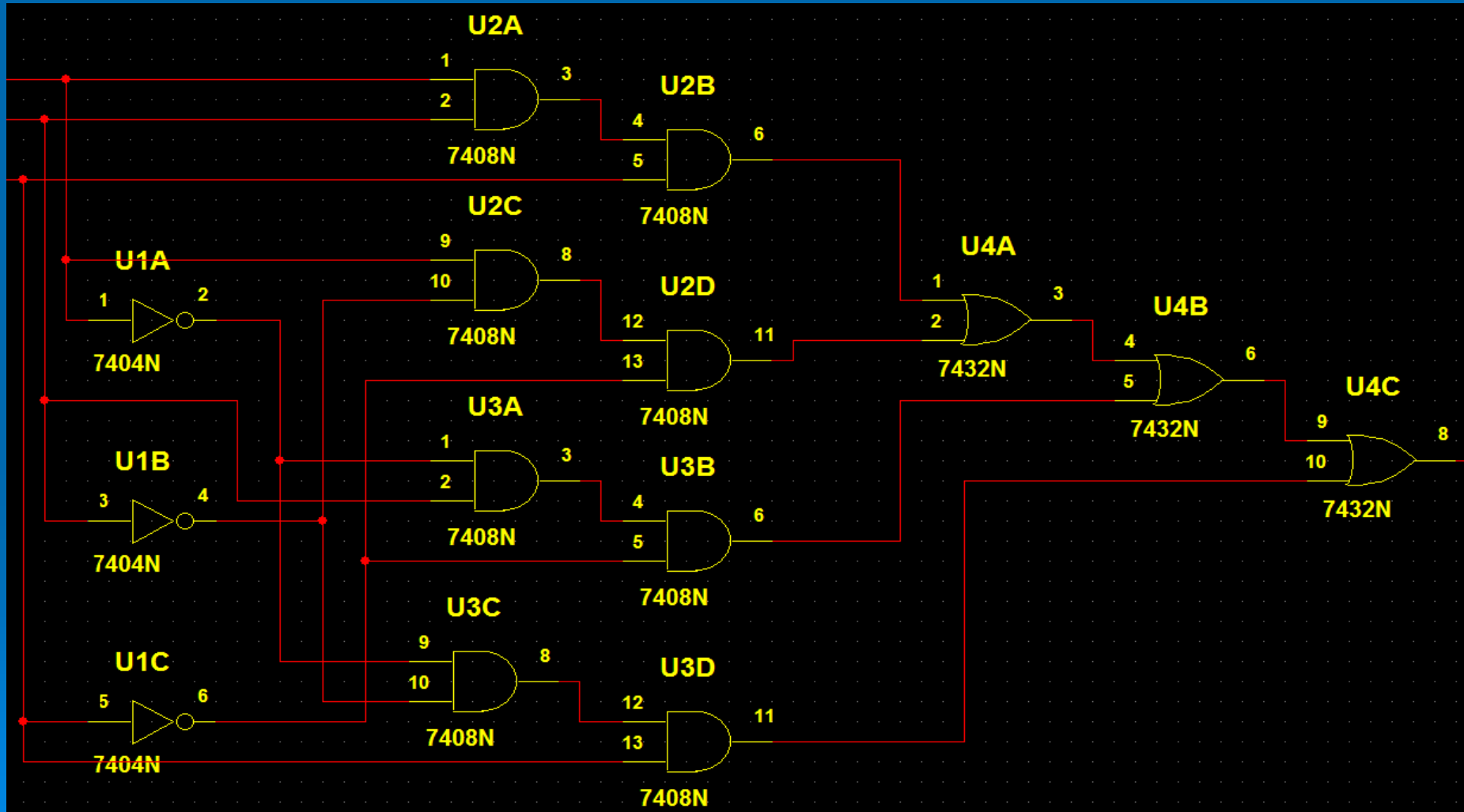
- List Report...
- Detail Report...
- Edit...

Buttons: OK, Cancel, Simple..., Help

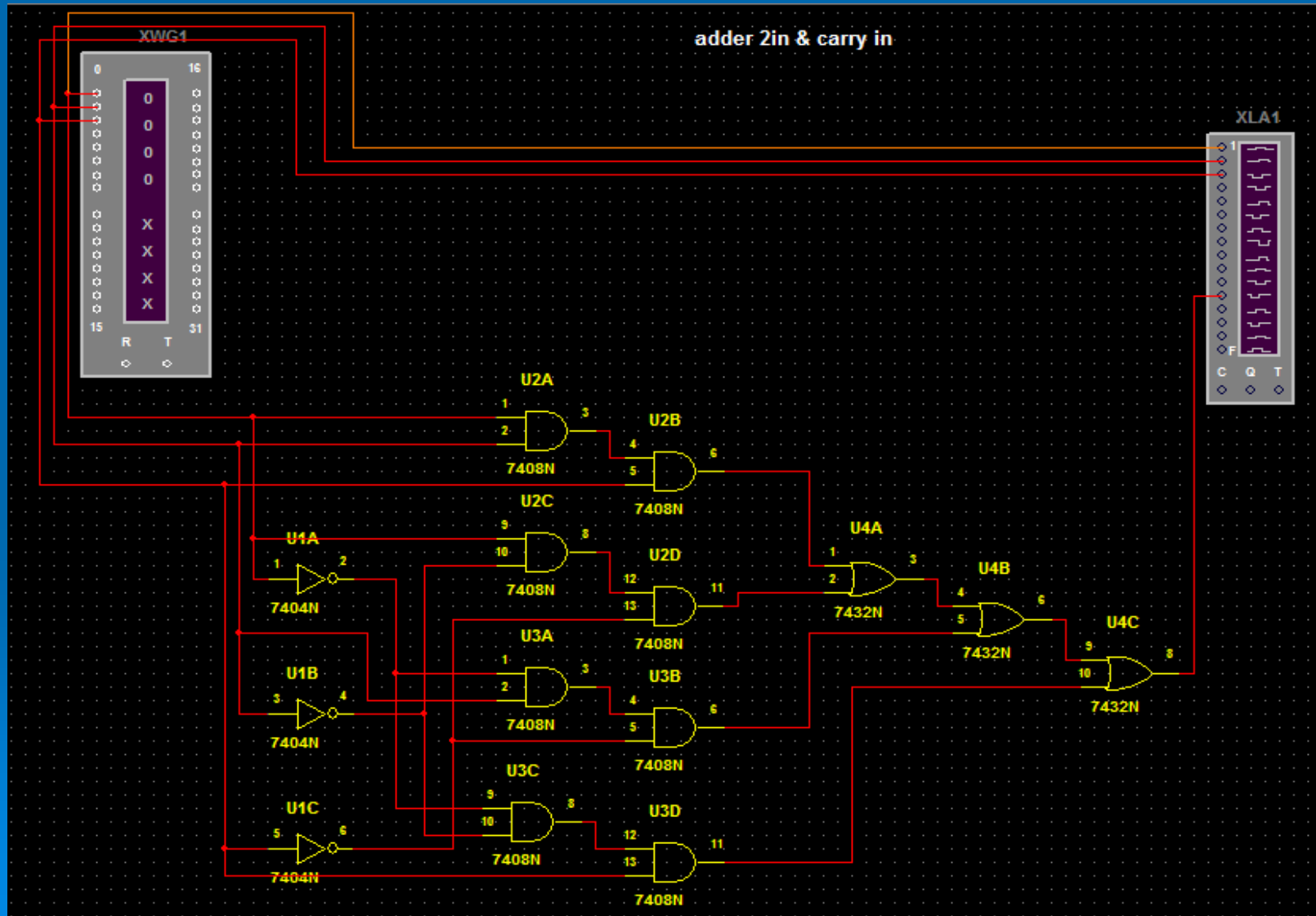
Electronics Workbench



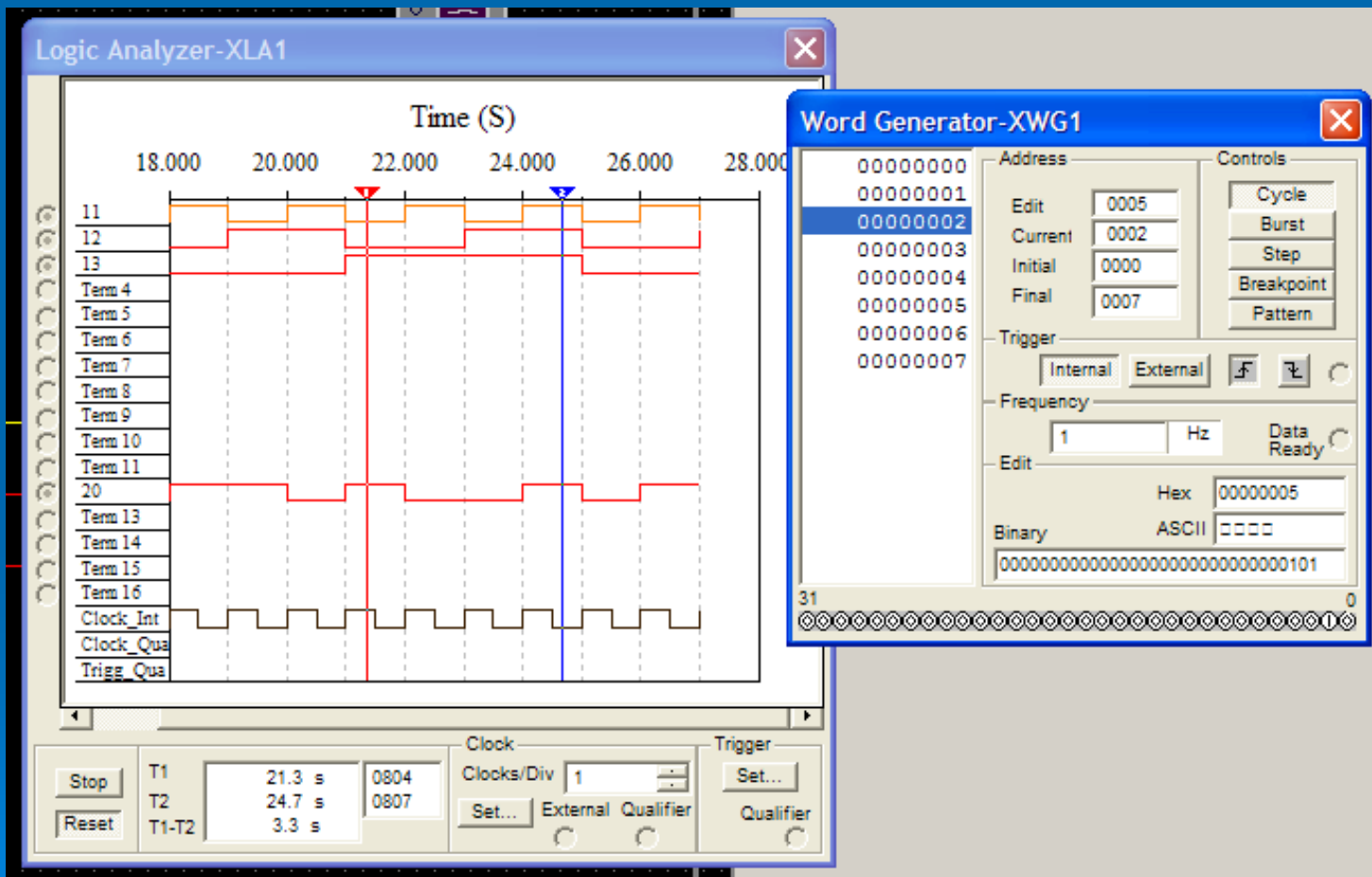
Electronics Workbench



Simulation



Simulation



WinCUPL

Atmel Corporation - Mozilla Firefox

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http://www.atmel.com/dyn/products/tools_card.asp?tool_id=2759

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WinCUPL

Description:

Atmel-WinCUPL is a complete and easy to use design software suitable for all Atmel SPLDs and CPLDs. It is supported on Win98, WinNT, Win2000, and WinXP platforms. Atmel-WinCUPL supports CUPL design entry, functional simulation, and includes the latest fitter technologies. To obtain your free copy of Atmel-WinCUPL, Version 5.30.4, just fill out our registration form, download, and install on the local drive of your PC. Note: If you have an older version of awincupl.exe or setupex.exe please re-download and then reinstall

Software:

	FIT5_0.ZIP Atmel WinCUPL Fitter File-Logic Doubling Versions Note: If you are currently using FIT5_0.Zip prior to rev 1.8.6.1 with Atmel WinCUPL version 5.2.16 this file is all you need to update. This ZIP file contains the latest versions of device fitters for all active Atmel CPLDs. These fitters work with Atmel-WinCUPL and Atmel ProChip Designer as well as Atmel-Synario V4.11 to optimally fit your logic design into a particular Atmel CPLD's available logic resources. Includes: FIT1502.EXE, FIT1504/EXE, and FIT1508.EXE support the ATF1502, ATF1504, and ATF1508 devices (includes Logic Doubling fitter technologies). FIT1500.EXE and FIND1500.EXE support ATF1500/A and also supports legacy tools Atmel-ABEL, Data I/OABEL and Atmel-ProPLD. FIT2500.EXE supports ATF2500 and ATF750 devices and supports legacy tools Atmel-ABEL 5.x and 6.0, Atmel-ProPLD and Viewlogic Workview Office 7.4x. ATMEL.STD (PLA) and APRIM.LIB (EDIF) Atmel ATF15xx Family primitive/device library.
Register to Download	Free! Atmel-WinCUPL with permanent license (20 MB) Includes: FIT5.0.ZIP, REV 1.8.7.8 Atmel-WinCUPL, Version 5.30.4 is suitable for Atmel SPLDs and CPLDs, and runs on Win98, WinNT, Win2000, and WinXP platforms. To obtain your free copy of Atmel-WinCUPL, Version 5.30.4, just fill out our registration form, download, and install on the local drive of your PC. Note: If you have an older dated version of awincupl.exe or setupex.exe please redownload and reinstall.

Advanced Search

WinCUPL expression

➤ $S = A'B'C + A'B'C' + A*B*C + A*B'C'$

➤ $A' = !A$ Inverter

➤ $A*B = A \& B$ And

➤ $A+B = A \# B$ Or

➤ $!a\&!b\&c \# !a\&b\&!c \# a\&b\&c \# a\&!b\&!c$

WinCUPL

The screenshot displays the WinCUPL software interface. The main window, titled "C:\WINCUPLE\EXAMPLES\ATMEL\ADD2.PLD", contains the following code:

```
Name      ADD2 ;
PartNo    00 ;
Date      10/1/2006 ;
Revision  01 ;
Designer  Vandikas I. ;
Company   EFARMOGI ;
Assembly  None ;
Location  Kozani;
Device    g20v8a ;

/* ***** INPUT PINS ***** */
PIN 1 = a;          /* */
PIN 2 = b;          /* */
PIN 3 = c;          /* */

/* ***** OUTPUT PINS ***** */
PIN 16 = sum;      /* */

/*
 * Logig : ADDER
 */

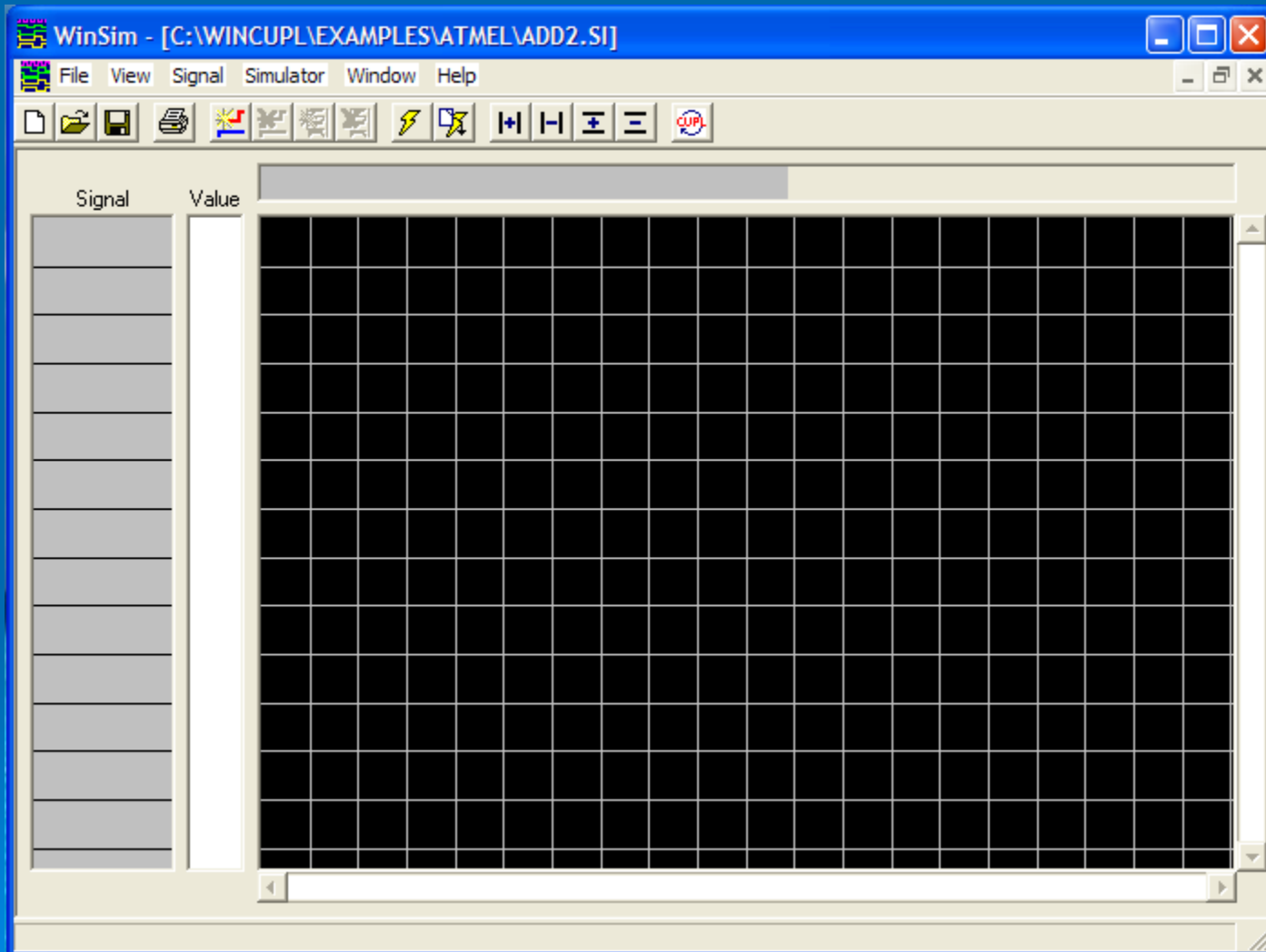
sum = !a & !b & c # !a & b & !c # a & b & c # a & !b & !c ;
```

The right-hand pane shows a project tree for "PROJECT: C:\WINCUPLE\...". The tree structure is as follows:

- C:\WINCUPLE\EXAMPLES\ATMEL\ADD2
 - ADD2.PLD
 - ADD2.abs
 - ADD2.jed
 - ADD2.pdf

The bottom status bar indicates "Line:7 Col:15" and includes checkboxes for "IN", "CAPS", "NUM", and "SCRL".

WinSIM



GAL (Generic Arrays Logic)

- 1986 from Lattice
- GAL20V8 include AND, OR, NOT
- OLMC (Output Logic Macro Cell)

GAL - ATF20V8

Features

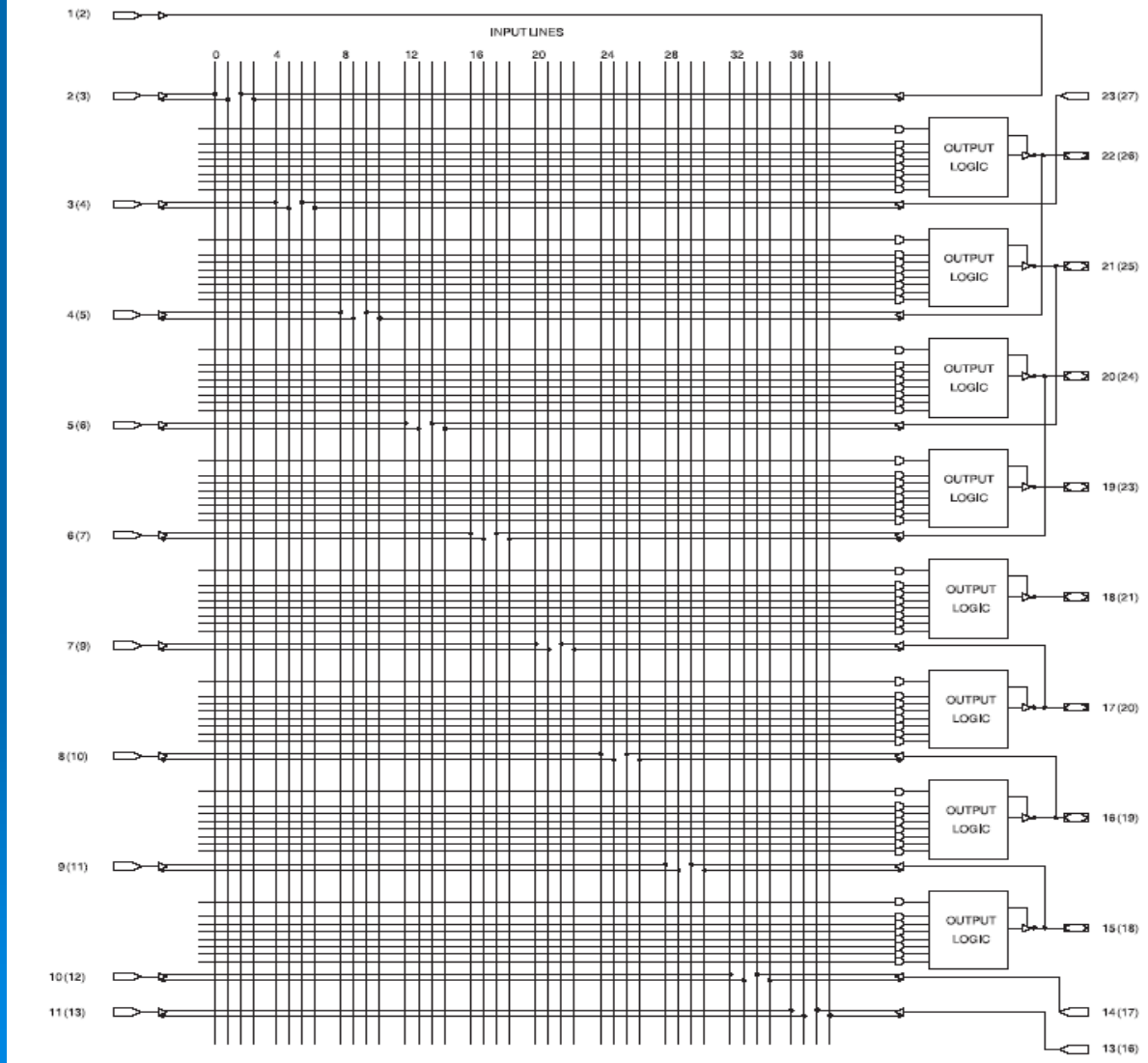
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Device	I _{CC} , Standby	I _{CC} , Active
ATF20V8B	50 mA	55 mA
ATF20V8BQ	35 mA	40 mA
ATF20V8BQL	5 mA	20 mA

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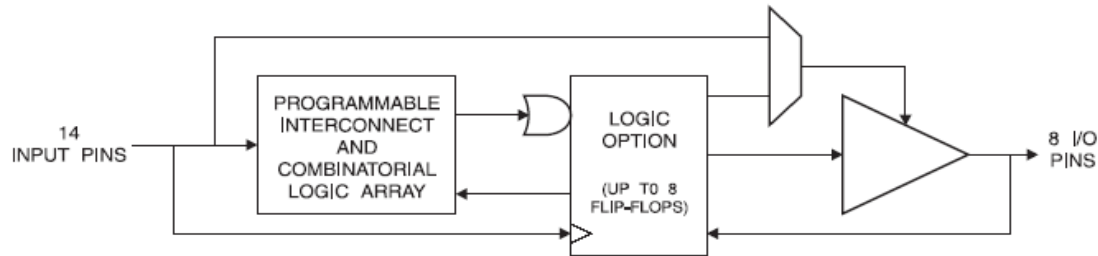
GAL - ATF20V8

Simple Mode Logic Diagram



GAL - ATF20V8

Block Diagram

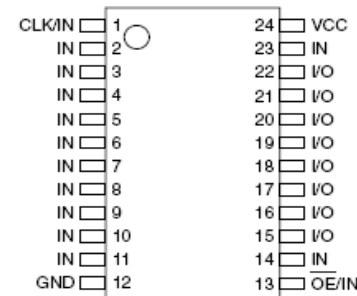


Pin Configurations

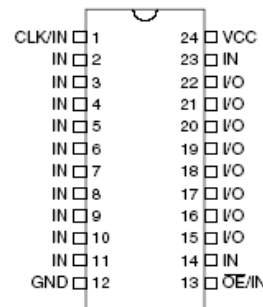
All Pinouts Top View

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bi-directional Buffers
OE	Output Enable
*	No Internal Connection
VCC	+5V Supply

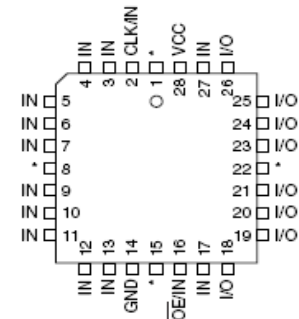
TSSOP



DIP/SOIC



PLCC



XELTEK programmer

http://www.xeltek-cn.com/sp580u.htm

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XELTEK programmer

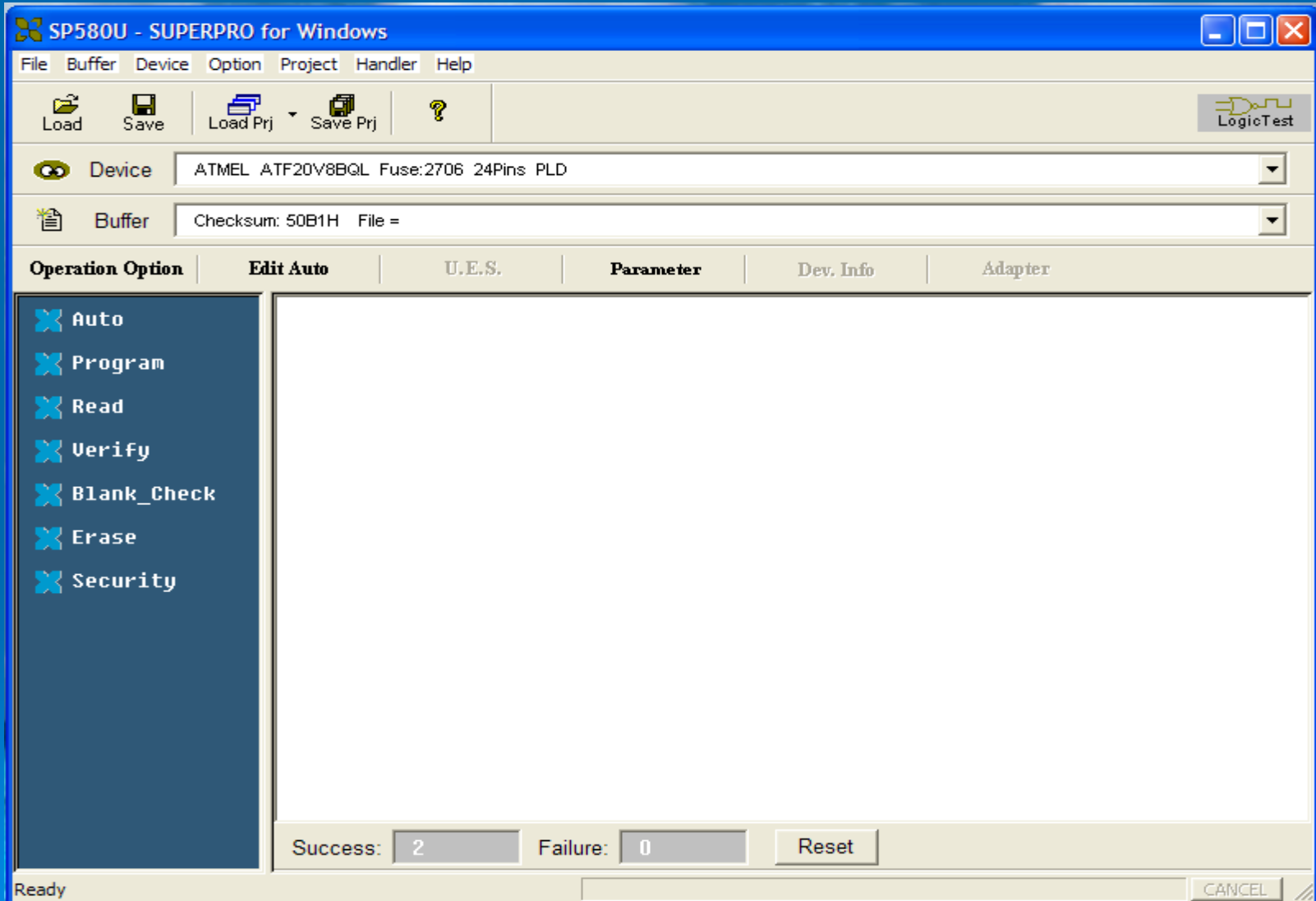
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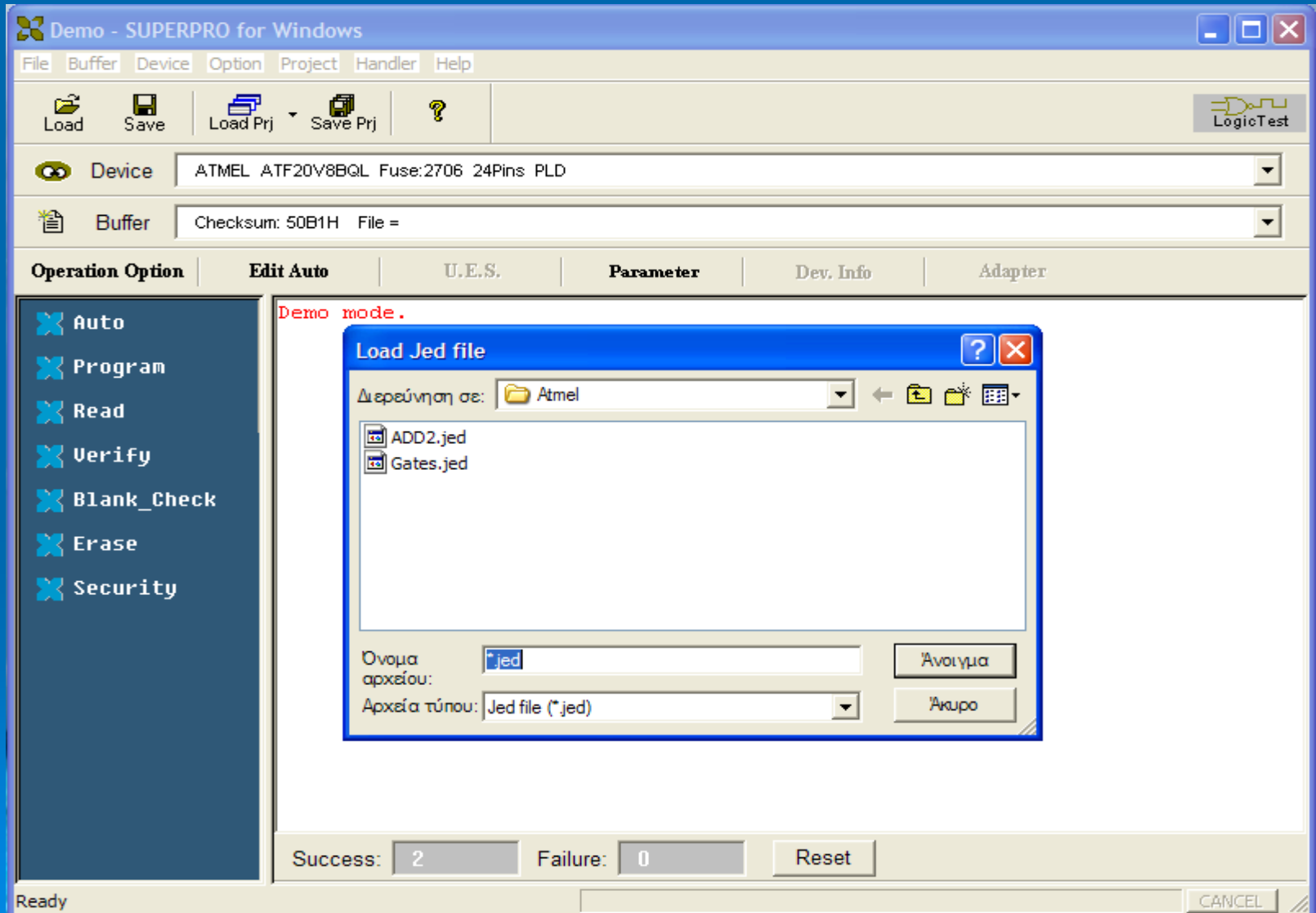
XELTEK programmer

1. Select Device
2. Blank_Check
3. Load file.jed
4. Program
5. Verify

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Programming with .jed file



Program

