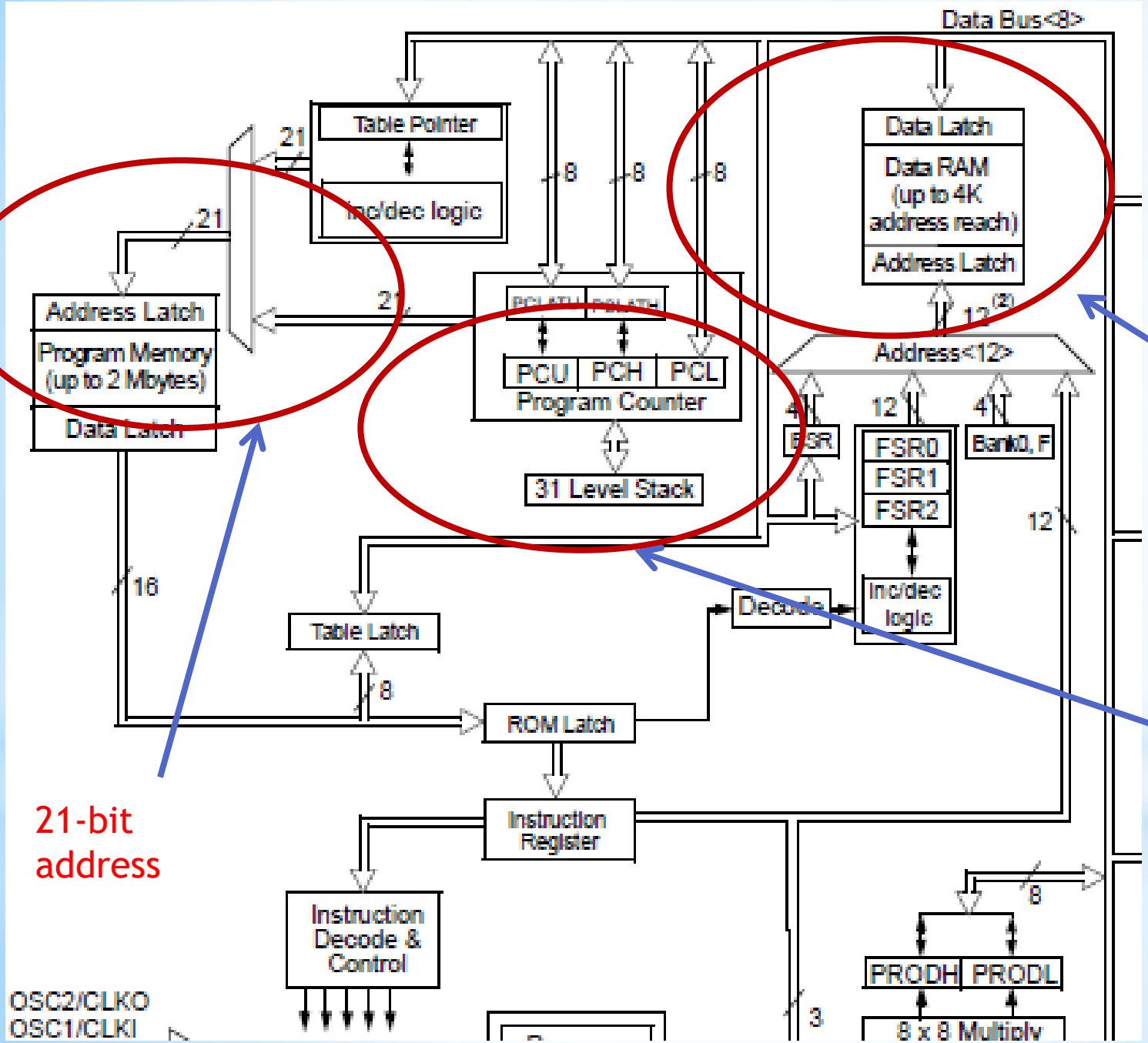
Οργάνωση μνήμης
Instruction Set
Interrupts
18F452

Οργάνωση Μνήμης

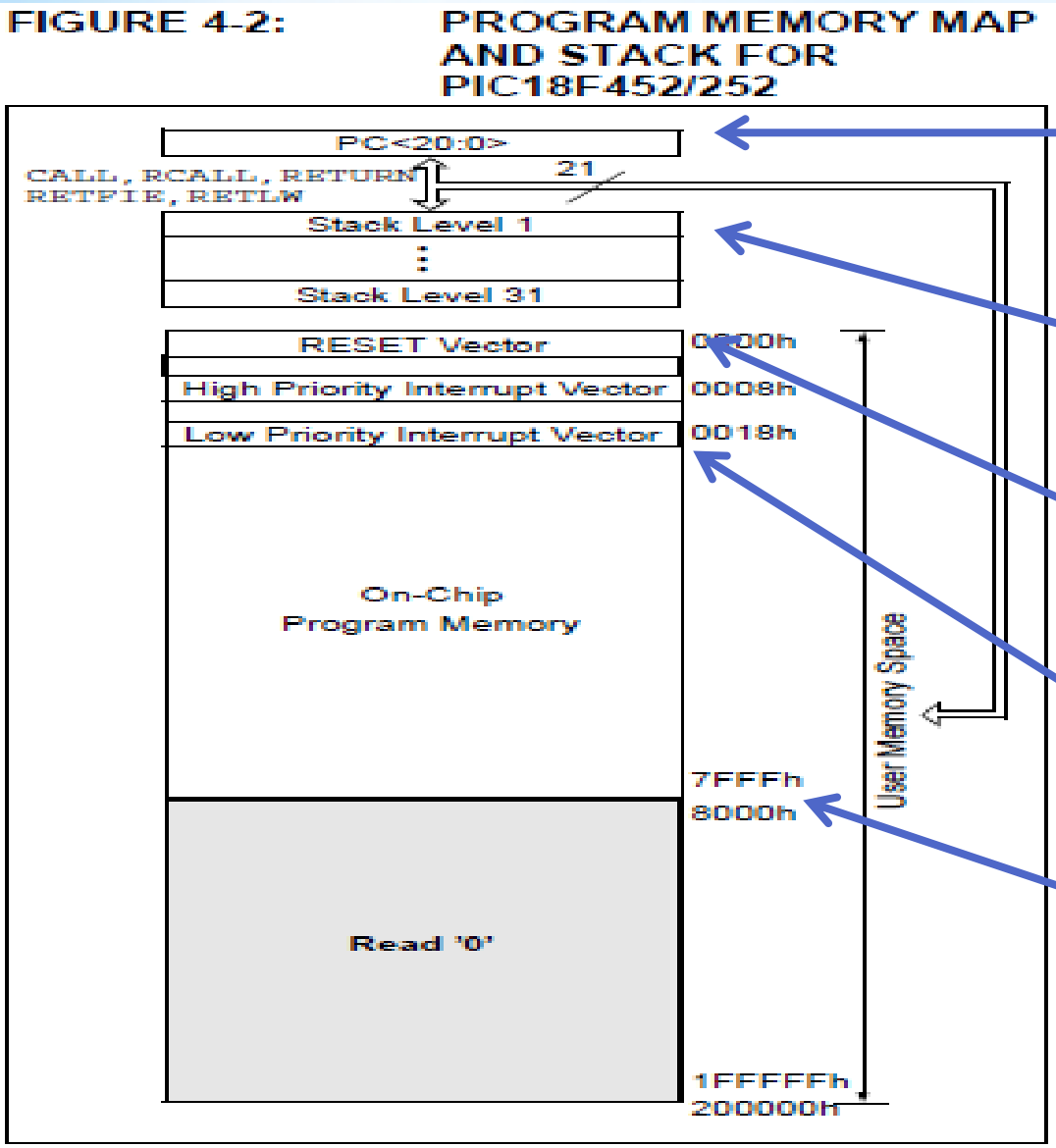
Τρία Μπλοκ Εσωτερικής Μνήμης

- Μνήμη Προγράμματος (Program Memory)
- Μνήμη Δεδομένων (Data RAM)
- Μη πτητική Μνήμη Δεδομένων (Data EEPROM)

Οι Μνήμες Προγράμματος και Δεδομένων χρησιμοποιούν διαφορετικούς διαύλους για να υπάρχει δυνατότητα ταυτόχρονης πρόσβασης


Data Bus<8>
Table Pointer
inc/dec logic
21
8
8
8
Data Latch
Data RAM
(up to 4K
address reach)
Address Latch
12
(2)
Address<12>
21
Address Latch
Program Memory
(up to 2 Mbytes)
Data Latch
PCU
PCH
PCL
Program Counter
31 Level Stack
4
12
4
BSR
FSR0
FSR1
FSR2
Bank0, F
12
16
Table Latch
Decode
Inc/dec
logic
8
ROM Latch
Instruction
Register
Instruction
Decode &
Control
8
PRODH
PRODL
8 x 8 Multiply
3
OSC2/CLKO
OSC1/CLKI
12-bit
address
21-bit
address
Program
counter
Stack
Pointer

Χάρτης Μνήμης Προγράμματος και Στοίβας



21-bit Program counter μπορεί να προσπελάσει μέχρι 2 Mbyte θέσεις Μνήμης

Η Στοίβα έχει βάθος 31 επίπεδα.(PUSH -POP)

Αρχική Διεύθυνση μετά από RESET
00000H

Δύο INTERRUPT vectors
00008H
00018H

On Chip FLASH Memory
32 KByte

Δείκτης Στοίβας (STACK POINTER)

STKPTR REGISTER

R/C-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STKOVF	STKUNF	—	SP4	SP3	SP2	SP1	SP0
bit 7							bit 0

Stack full bit

Stack underflow bit

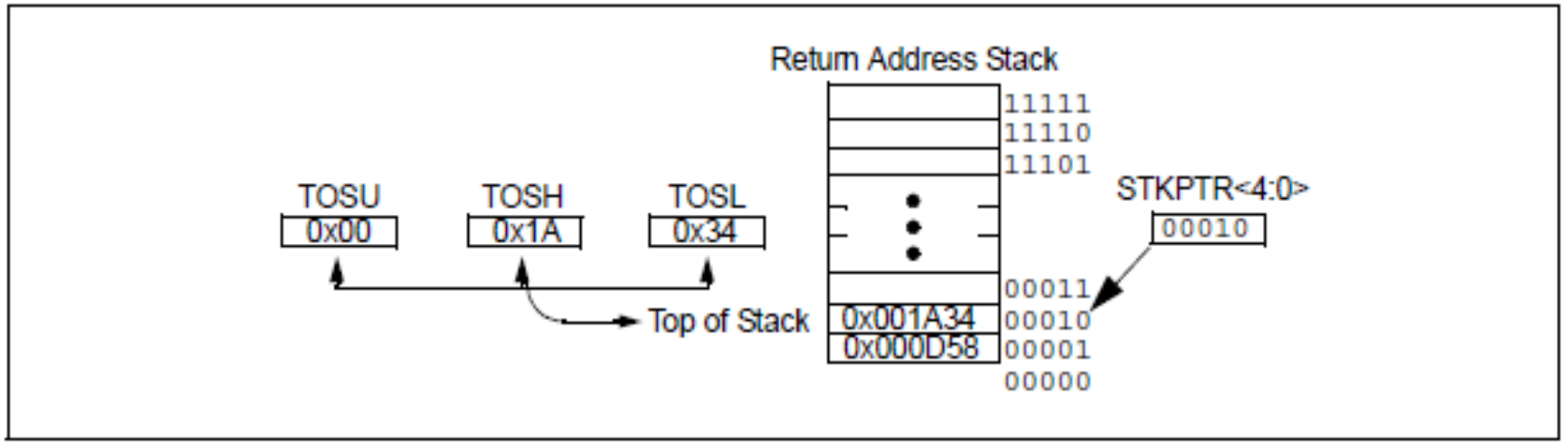
Τρέχουσα τιμή στοίβας

Αυξάνει με PUSH

Μειώνεται με POP

Στοίβα και σχετιζόμενοι καταχωρητές

FIGURE 4-3: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS



Η Στοίβα έχει βαθος 31 επίπεδα και εύρος 21 bit.

Τρεις καταχωρητές TOSU, TOSH, TOSL έχουν τα περιεχόμενα της κορυφής της στοίβας.

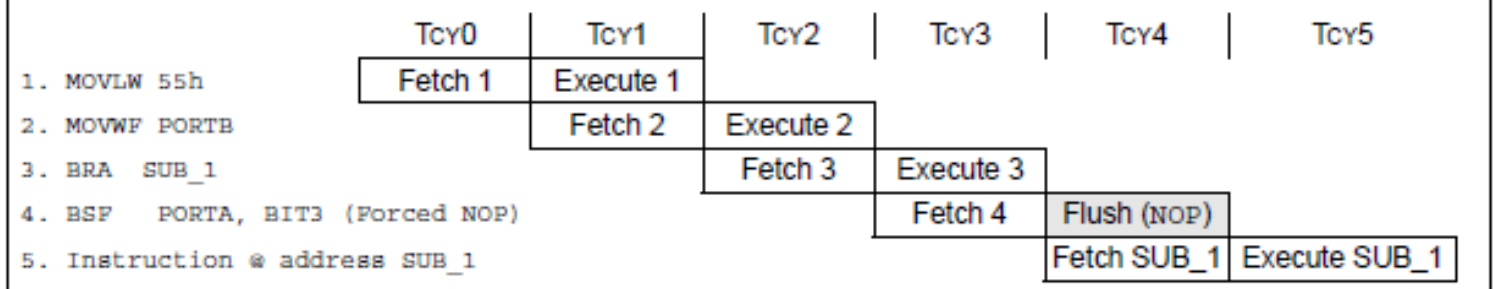
Μορφή και εκτέλεση εντολών

Οι Εντολές αποθηκεύονται στη μνήμη Προγράμματος σε 2 ή 4 συνεχόμενα Bytes.

Ο μετρητής προγράμματος (PC) αυξάνει πάντα κατά δυο.

Για την αποδοτικότερη λειτουργία του επεξεργαστή οι εντολές εκτελούνται σε pipeline.

EXAMPLE 4-2: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

Παράδειγμα αποθήκευσης εντολών στην Μνήμη Προγράμματος

FIGURE 4-5: INSTRUCTIONS IN PROGRAM MEMORY

			Program Memory Byte Locations → LSB = 1	LSB = 0	Word Address ↓
					000000h
					000002h
					000004h
					000006h
Instruction 1:	MOVLW	055h	0Fh	55h	000008h
Instruction 2:	GOTO	000006h	EFh	03h	00000Ah
			F0h	00h	00000Ch
Instruction 3:	MOVFF	123h, 456h	C1h	23h	00000Eh
			F4h	56h	000010h
					000012h
					000014h

EXAMPLE 4-3: TWO-WORD INSTRUCTIONS

CASE 1:

Object Code	Source Code		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; No, execute 2-word instruction
1111 0100 0101 0110			; 2nd operand holds address of REG2
0010 0100 0000 0000	ADDWF	REG3	; continue code

CASE 2:

Object Code	Source Code		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; Yes
1111 0100 0101 0110			; 2nd operand becomes NOP
0010 0100 0000 0000	ADDWF	REG3	; continue code

Παράδειγμα (πηγαίος κώδικας)

```
char temp, temp1;

 void main(){
      TRISB =0xFF;
      TRISC =0x00;

      temp=18;
      temp1 = temp+PORTB;

 }
```

Παράδειγμα (assembly και μνήμη προγράμματος)

```
; ADDRESS OPCODE     ASM
; ------------------------------------------
$0000     $EF04     F000                GOTO      _main
$0008     $         _main:
;memory_map.c,3 ::            void main(){
;memory_map.c,5 ::            TRISB =0xFF;
$0008     $0EFF                         MOVLW     255
$000A     $6E93                         MOVWF     TRISB, 0
;memory_map.c,6 ::            TRISC =0x00;
$000C     $6A94                         CLRF      TRISC, 0
;memory_map.c,8 ::            temp=18;
$000E     $0E12                         MOVLW     18
$0010     $6E15                         MOVWF     _temp, 0
;memory_map.c,9 ::            temp1 = temp+PORTB;
$0012     $5081                         MOVF      PORTB, 0, 0
$0014     $0F12                         ADDLW     18
$0016     $6E16                         MOVWF     _temp1, 0
;memory_map.c,13 ::           }
$0018     $D7FF                         BRA       $

//** Procedures locations **
//ADDRESS           PROCEDURE
//------------------------------------------
$0008               main
```

GOTO	Unconditional Branch			
Syntax:	[*label*] GOTO k			
Operands:	$0 \le k \le 1048575$			
Operation:	$k \rightarrow PC<20:1>$			
Status Affected:	None			
Encoding:				
1st word (k<7:0>)	1110	1111	k_7kkk	$kkkk_0$
2nd word(k<19:8>)	1111	$k_{19}kkk$	kkkk	$kkkk_8$
Description:	GOTO allows an unconditional branch anywhere within entire 2 Mbyte memory range. The 20-bit value 'k' is loaded into PC<20:1>. GOTO is always a two-cycle instruction.			

MOVLW	Move literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	$k \rightarrow W$
Status Affected:	None
Encoding:	0000 1110 kkkk kkkk
Description:	The eight-bit literal 'k' is loaded into W.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f [,a]
Operands:	$0 \le f \le 255$ $a \in [0,1]$
Operation:	(W) $\rightarrow$ f
Status Affected:	None
Encoding:	0110 111a ffff ffff
Description:	Move data from W to register 'f'. Location 'f' can be anywhere in the 256 byte bank. If 'a' is 0, the Access Bank will be selected, over-riding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).

Παράδειγμα (μνήμη δεδομένων)

```
//** Variables locations **
//ADDRESS                 VARIABLE
//-----------------------------------------
$0000                     STACK_0
$0001                     STACK_1
$0002                     STACK_2
$0003                     STACK_3
.............
$0012                     STACK_18
$0013                     STACK_19
$0014                     STACK_20
$0015                     _temp
$0016                     _temp1
$0F81                     PORTB
$0F93                     TRISB
$0F94                     TRISC
```

Αρχείο HEX με εκτελεσιμο κώδικα

```
:10000000 04EF00F0FFFFFFFFFF0E936E946A120EE5
:10001000 156E8150120F166EFFD7FFFFFFFFFFFF17
:020000040030CA
:0E000000FFFAFFFEFFFFFBFFFFFFFFFFFFFF0A
:00000001FF
```

Παράδειγμα κώδικα εγγραφής σε και ανάγνωσης από FLASH

```
unsigned short i = 0, j = 0;
unsigned  short addr;
unsigned short dataRd;
unsigned short dataWr[64] =
          {1,2,3,4,5,6,7,8,9,0,1,2,3,4,5,6,7,8,9,0,
           1,2,3,4,5,6,7,8,9,0,1,2,3,4,5,6,7,8,9,0,
           1,2,3,4,5,6,7,8,9,0,1,2,3,4,5,6,7,8,9,0,
           1,2,3,4};

void main() {
  ADCON1 = 0x0F;              // configure AN pins as digital
  PORTB = 0;
  TRISB = 0;
  addr = 0x00000A30;          // valid for P18F452
  Flash_Erase_Write_64(addr, dataWr);
  addr = 0x00000A30;
  for (i = 0; i < 64; i++) {
    dataRd = Flash_Read(addr++);
    PORTB = dataRd;
    Delay_ms(500);
  }
}//~!
```

```
; ADDRESS             OPCODE              ASM
; ------------------------------------------
$0000                 $EF13               F000                                                GOTO                _main
$0008                 $                   _Flash_Read:
;Flash_w8_e64.c,113 ::
;Flash_w8_e64.c,115 ::
$0008                 $C01C               FFF6                                                MOVFF               FARG_Flash_Read+0, TBLPTRL
;Flash_w8_e64.c,116 ::
$000C                 $C01D               FFF7                                                MOVFF               FARG_Flash_Read+1, TBLPTRH
;Flash_w8_e64.c,117 ::
$0010                 $C01E               FFF8                                                MOVFF               FARG_Flash_Read+2, TBLPTRU
;Flash_w8_e64.c,118 ::
$0014                 $0008                                                                   TBLRD*
;Flash_w8_e64.c,119 ::
$0016                 $CFF5               F000                                                MOVFF               TABLAT, STACK_0
;Flash_w8_e64.c,120 ::
$001A                 $0012                                                                   RETURN
$001C                 $                   GlobalIniflash_access:
$001C                 $0E00                                                                   MOVLW               0
$001E                 $6E15                                                                   MOVWF               _i+0, 0
$0020                 $0E00                                                                   MOVLW               0
$0022                 $6E16                                                                   MOVWF               _j+0, 0
;flash_access.c,1 ::                                       unsigned short i = 0, j = 0;
$0024                 $0012                                                                   RETURN
$0026                 $                   _main:
;flash_access.c,5 ::                                       void main() {
;flash_access.c,14 ::                                      addr = 0x0000000;
$0026                 $EC0E               F000                                                CALL                GlobalIniflash_access
$002A                 $6A17                                                                   CLRF                _addr, 0
$002C                 $6A18                                                                   CLRF                _addr+1, 0
$002E                 $6A19                                                                   CLRF                _addr+2, 0
$0030                 $6A1A                                                                   CLRF                _addr+3, 0
;flash_access.c,15 ::                                      dataRd = Flash_Read(addr);
$0032                 $6A1C                                                                   CLRF                FARG_Flash_Read+0, 0
$0034                 $6A1D                                                                   CLRF                FARG_Flash_Read+1, 0
$0036                 $6A1E                                                                   CLRF                FARG_Flash_Read+2, 0
$0038                 $6A1F                                                                   CLRF                FARG_Flash_Read+3, 0
$003A                 $EC04               F000                                                CALL                _Flash_Read
$003E                 $C000               F01B                                                MOVFF               STACK_0, _dataRd
;flash_access.c,25 ::                                      }//~!
$0042                 $D7FF                                                                   BRA                 $
```

Οργάνωση Μνήμης Δεδομένων

* Η μνήμη δεδομένων είναι υλοποιημένη ως στατική RAM.

* Κάθε θέση μνήμης προσδιορίζεται με 12-bit διεύθυνση επιτρέποντας μέχρι 4096 byte μνήμης.

* Η μνήμη είναι διαιρεμένη σε 16 τμήματα (banks) των 256 bytes. Τέσσερα bit ενός καταχωρητή (BSR) καθορίζουν το τμήμα.

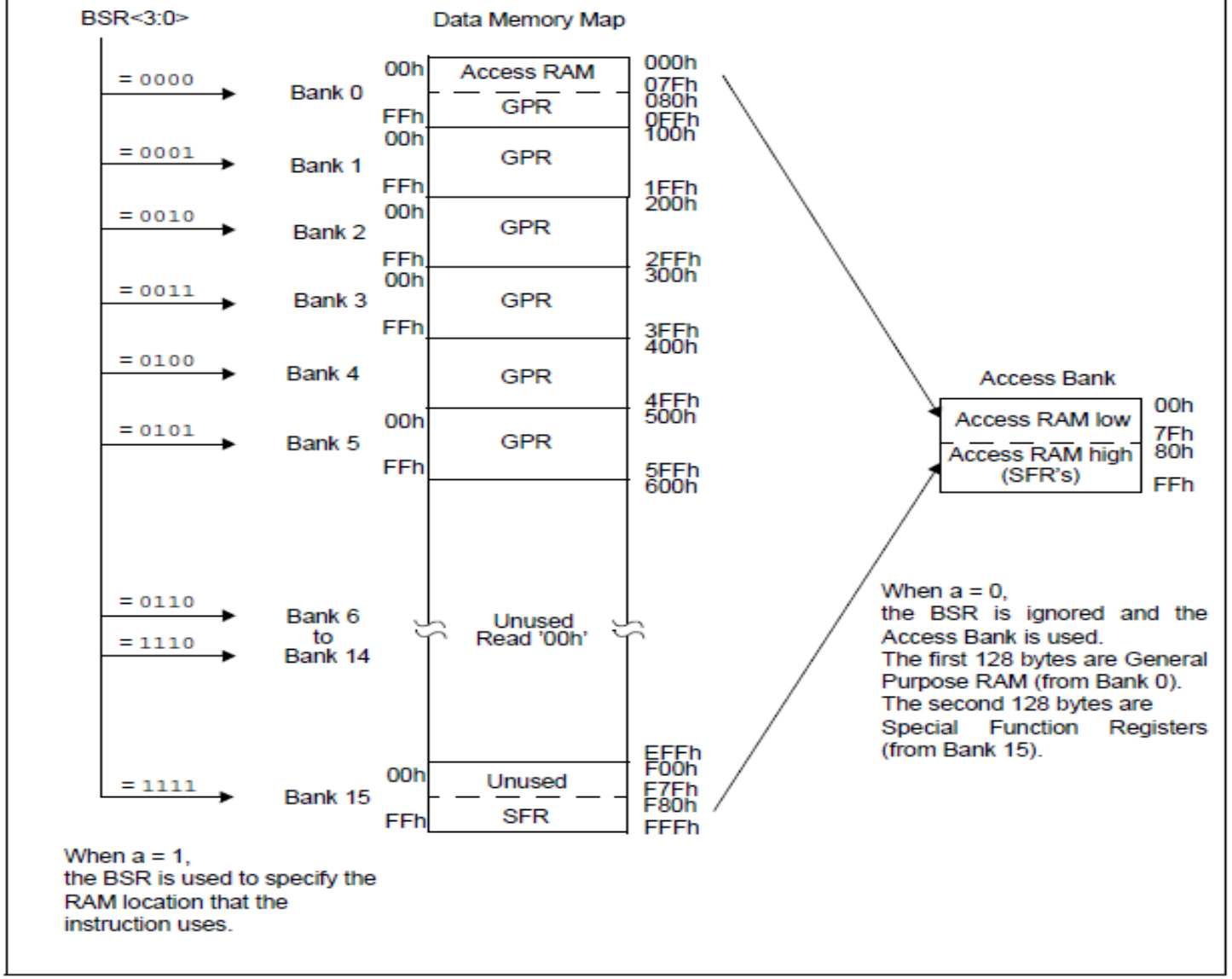
* Η Μνήμη δεδομένων περιλαμβάνει Καταχωρητές ειδικής Λειτουργίας (Special Function Registers) που χρησιμεύουν για έλεγχο του μικροελεγτή και περιφερειακών λειτουργιών.

* Οι SFR στις τελευταίες διευθύνσεις της 15^{ης} ομάδας μνήμης.

* Οι υπόλοιπες θεσεις μνήμης μπορούν να χρησιμοποιηθούν ως Γενικοί Καταχωρητές (GPR)

Οργάνωση Μνήμης Δεδομένων

FIGURE 4-7: DATA MEMORY MAP FOR PIC18F252/452



Πίνακας καταχωρητών ειδικού σκοπού

TABLE 4-1: SPECIAL FUNCTION REGISTER MAP

Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2(3)	FBFh	CCPR1H	F9Fh	IPR1
FFEh	TOSH	FDEh	POSTINC2(3)	FBEh	CCPR1L	F9Eh	PIR1
FFDh	TOSL	FDDh	POSTDEC2(3)	FBDh	CCP1CON	F9Dh	PIE1
FFCh	STKPTR	FDCh	PREINC2(3)	FBCh	CCPR2H	F9Ch	—
FFBh	PCLATU	FDBh	PLUSW2(3)	FBBh	CCPR2L	F9Bh	—
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	—
FF9h	PCL	FD9h	FSR2L	FB9h	—	F99h	—
FF8h	TBLPTRU	FD8h	STATUS	FB8h	—	F98h	—
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	—	F97h	—
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	—	F96h	TRISE(2)
FF5h	TABLAT	FD5h	T0CON	FB5h	—	F95h	TRISD(2)
FF4h	PRODH	FD4h	—	FB4h	—	F94h	TRISC
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB
FF2h	INTCON	FD2h	LVDCON	FB2h	TMR3L	F92h	TRISA
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	—
FF0h	INTCON3	FD0h	RCON	FB0h	—	F90h	—
FEFh	INDF0(3)	FCFh	TMR1H	FAFh	SPBRG	F8Fh	—
FEEh	POSTINC0(3)	FCEh	TMR1L	FAEh	RCREG	F8Eh	—
FEDh	POSTDEC0(3)	FCDh	T1CON	FADh	TXREG	F8Dh	LATE(2)
FECh	PREINC0(3)	FCCh	TMR2	FACh	TXSTA	F8Ch	LATD(2)
FEBh	PLUSW0(3)	FCBh	PR2	FABh	RCSTA	F8Bh	LATC
FEAh	FSR0H	FCAh	T2CON	FAAh	—	F8Ah	LATB
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	—
FE7h	INDF1(3)	FC7h	SSPSTAT	FA7h	EECON2	F87h	—
FE6h	POSTINC1(3)	FC6h	SSPCON1	FA6h	EECON1	F86h	—
FE5h	POSTDEC1(3)	FC5h	SSPCON2	FA5h	—	F85h	—
FE4h	PREINC1(3)	FC4h	ADRESH	FA4h	—	F84h	PORTE(2)
FE3h	PLUSW1(3)	FC3h	ADRESL	FA3h	—	F83h	PORTD(2)
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB
FE0h	BSR	FC0h	—	FA0h	PIE2	F80h	PORTA

EEPROM ΜΝΗΜΗ ΔΕΔΟΜΕΝΩΝ

Η EERPOM δεδομένων είναι αναγνώσιμη και εγγράψιμη κατά την λειτουργία του μικροελεγκτή.

Δεν είναι προσβάσιμη στον χώρο της RAM αλλά μπορεί να προσπελαστεί έμμεσα μέσω καταχωρητών ειδικού σκοπού:

EECON1

EECON2

EEDATA → 8-bit δεδομένα EEPROM

EEADR -> 8-bit διεύθυνση EEPROM

EEPROM ΜΝΗΜΗ ΔΕΔΟΜΕΝΩΝ

EXAMPLE 6-1: DATA EEPROM READ

```
        MOVLW   DATA_EE_ADDR    ;
        MOVWF   EEADR           ; Data Memory Address to read
        BCF     EECON1, EEPGD   ; Point to DATA memory
        BCF     EECON1, CFGS    ; Access program FLASH or Data EEPROM memory
        BSF     EECON1, RD      ; EEPROM Read
        MOVF    EEDATA, W       ; W = EEDATA
```

EXAMPLE 6-2: DATA EEPROM WRITE

```
                MOVLW   DATA_EE_ADDR    ;
                MOVWF   EEADR           ; Data Memory Address to read
                MOVLW   DATA_EE_DATA    ;
                MOVWF   EEDATA          ; Data Memory Value to write
                BCF     EECON1, EEPGD   ; Point to DATA memory
                BCF     EECON1, CFGS    ; Access program FLASH or Data EEPROM memory
                BSF     EECON1, WREN    ; Enable writes

                BCF     INTCON, GIE     ; Disable interrupts
  Required      MOVLW   55h             ;
  Sequence      MOVWF   EECON2          ; Write 55h
                MOVLW   AAh             ;
                MOVWF   EECON2          ; Write AAh
                BSF     EECON1, WR      ; Set WR bit to begin write
                BSF     INTCON, GIE     ; Enable interrupts

                .                       ; user code execution
                .
                .
                BCF     EECON1, WREN    ; Disable writes on write complete (EEIF set)
```

ΠΑΡΑΔΕΙΓΜΑ ΕΓΓΡΑΦΗΣ ΚΑΙ ΑΝΑΓΝΩΣΗΣ ΑΠΌ EEPROM

```
unsigned short i = 0, j = 0;

void main() {
  PORTB = 0;
  TRISB = 0;

  j = 4;
  for (i = 0; i < 20u; i++)
    EEprom_Write(i, j++);

  for (i = 0; i < 20u; i++) {
    PORTB = EEprom_Read(i);
    Delay_ms(500);
  }
}//~!
```

```
; ADDRESS       OPCODE          ASM
; ----------------------------------------------
$0000           $EF25           F000                    GOTO            _main
$0008           $               _Eeprom_Write:
$0008           $               L_Eeprom_Write_0:
$0008           $A2A6                                   BTFSS           EECON1, 1, 0
$000A           $D002                                   BRA             L_Eeprom_Write_1
$000C           $0000                                   NOP
$000E           $D7FC                                   BRA             L_Eeprom_Write_0
$0010           $               L_Eeprom_Write_1:
$0010           $9CA6                                   BCF             EECON1, 6, 0
$0012           $C017           FFA9                    MOVFF           FARG_Eeprom_Write+0, EEADR
$0016           $C018           FFA8                    MOVFF           FARG_Eeprom_Write+1, EEDATA
$001A           $9EA6                                   BCF             EECON1, 7, 0
$001C           $84A6                                   BSF             EECON1, 2, 0
$001E           $9EF2                                   BCF             INTCON, 7, 0
$0020           $0E55                                   MOVLW           85
$0022           $6EA7                                   MOVWF           EECON2, 0
$0024           $0EAA                                   MOVLW           170
$0026           $6EA7                                   MOVWF           EECON2, 0
$0028           $82A6                                   BSF             EECON1, 1, 0
$002A           $8EF2                                   BSF             INTCON, 7, 0
$002C           $94A6                                   BCF             EECON1, 2, 0
$002E           $0012                                   RETURN
$0030           $               _Eeprom_Read:
$0030           $9CA6                                   BCF             EECON1, 6, 0
$0032           $C017           FFA9                    MOVFF           FARG_Eeprom_Read+0, EEADR
$0036           $9EA6                                   BCF             EECON1, 7, 0
$0038           $80A6                                   BSF             EECON1, 0, 0
$003A           $CFA8           F000                    MOVFF           EEDATA, STACK_0
$003E           $0012                                   RETURN
```

Interrupts (Διακοπές)

Οι PIC18FXX2 έχουν πολλαπλές πηγές Interrupt και μια ιεράρχηση που επιτρέπει σε κάθε διακοπή να έχει υψηλή ή χαμηλή προτεραιότητα.

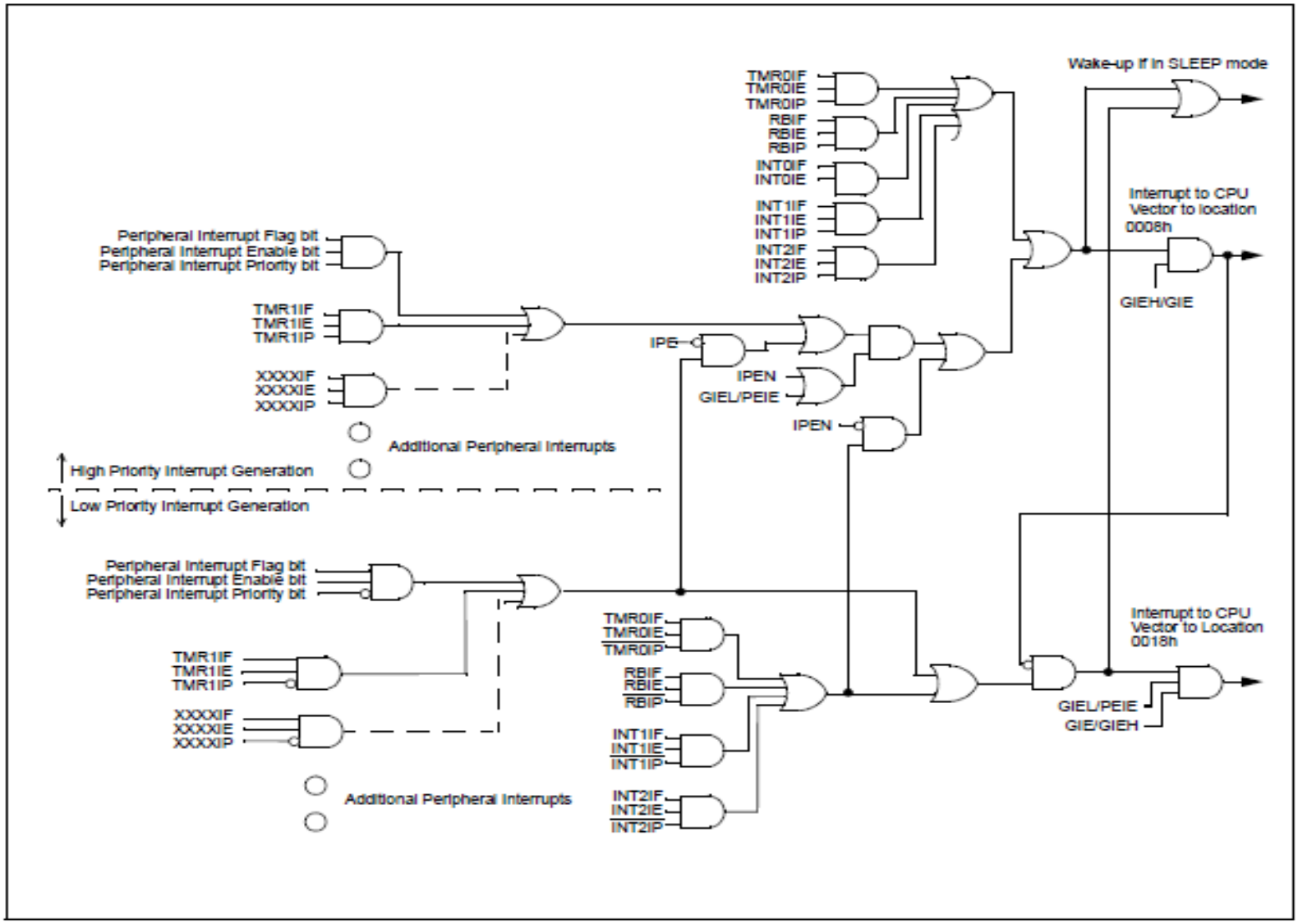
Οι Διακοπές υψηλής προτεραιότητας χρησιμοποιούν την θέση 000008H και οι χαμηλής προτεραιότητας την θέση 000018H.

Δέκα καταχωρητές χρησιμοποιούνται για την διαχείριση των διακοπών.

- RCON
- INTCON
- INTCON2
- INTCON3
- PIR1,PIR2
- PIE1,PIE2
- IPR1, IPR2

Λογικό Διάγραμμα Interrupts

FIGURE 8-1: INTERRUPT LOGIC



Ενδεικτικές πηγές Interrupt

RB0/INT0 -> εξωτερικό interrupt υψηλής προτεραιότητας

PB1/INT1 ->εξωτερικά interrupt ρυθμιζόμενης

PB2/INT2 προτεραιότητας

TIMER0 -> εσωτερικό Interrupt ρυθμιζόμενης προτεραιότητας

PORTB -> εξωτερικό Interrupt όταν συμβεί αλλαγή στα pin RB4-RB7

Interrupt Service Routine

Κώδικας που τοποθετείται στην καθορισμένη θέση μνήμης (interrupt vector) και περιέχει τις ενέργειες που θέλουμε να εκτελέσει ο μικροελεγτής όταν συμβεί μια διακοπή.

Void interrupt() → στην θεση 0008H

Void interrupt_low() ->στη θεση 0018H

Interrupt Service Routine

Interrupts can be easily handled by means of reserved word interrupt. mikroC implictly declares function interrupt which cannot be redeclared. Its prototype is:

void interrupt(void);For P18 low priority interrupts reserved word is interrupt_low:

void interrupt_low(void);You are expected to write your own definition (function body) to handle interrupts in your application.

mikroC saves the following SFR on stack when entering interrupt and pops them back upon return:

PIC12 family: W, STATUS, FSR, PCLATH

PIC16 family: W, STATUS, FSR, PCLATH

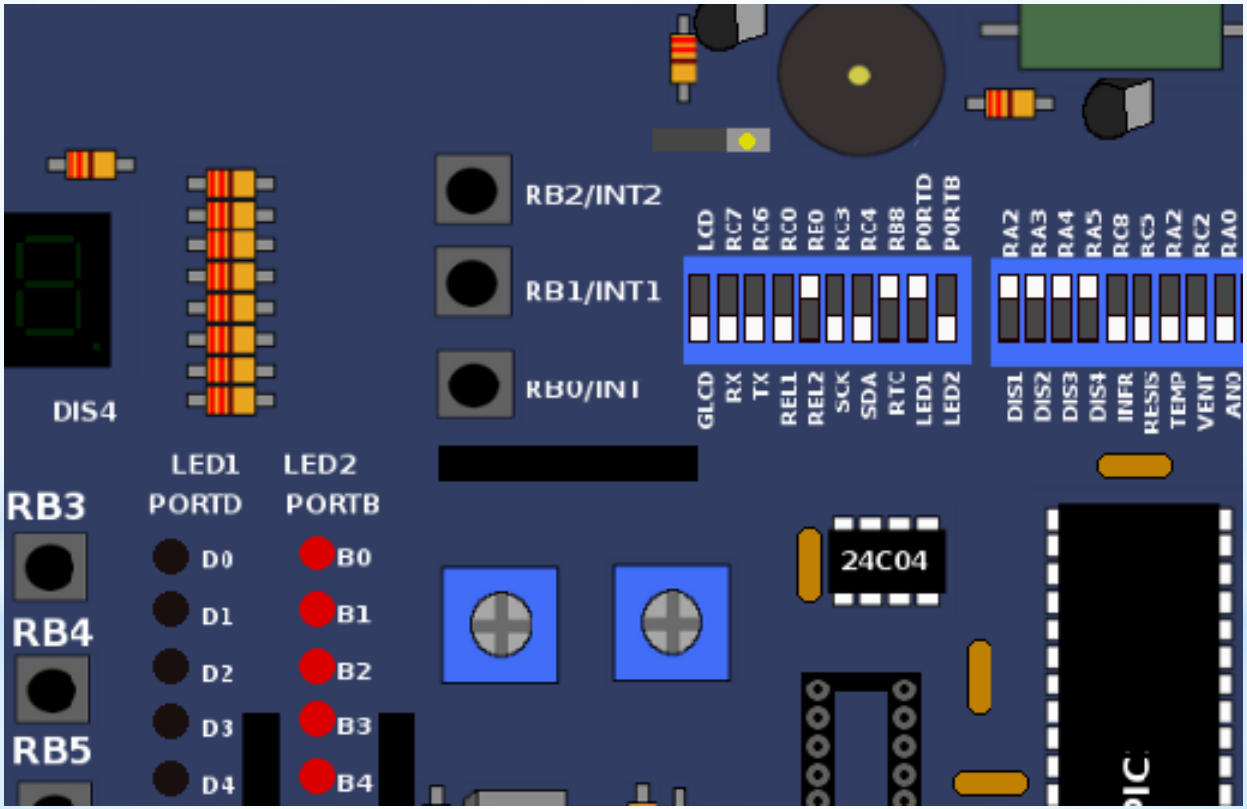
PIC18 family: FSR (fast context is used to save WREG, STATUS, BSR)

Παράδειγμα Interrupt Service Routine

```
void interrupt() {
  if (INTCON.TMR0IF) {
            counter++;
            TMR0 = 96;
            INTCON.TMR0F = 0;
  }
  else if (INTCON.RBIF) {
            counter++;
            TMR0 = 96;
            INTCON.RBIF = 0;
  }
}
```

Παράδειγμα χρήσης INTERRUPT

Χρήση των interrupt INT0 και INT1 για την ενεργοποίηση του ρελέ 1 στην εικονική πλακέτα ενώ εκτελείται κάποια άλλη λειτουργία στον μικροελεγκτή.



Interrupt Registers (1)

REGISTER 8-1: INTCON REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

INTCON = 0b11010000;

bit 7 **GIE/GIEH:** Global Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts
When IPEN = 1:
1 = Enables all high priority interrupts
0 = Disables all interrupts

bit 6 **PEIE/GIEL:** Peripheral Interrupt Enable bit
When IPEN = 0:
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
When IPEN = 1:
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4 **INT0IE:** INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 3 **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INT0IF:** INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0 **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note: A mismatch condition will continue to set this bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared.

Interrupt Registers (2)

REGISTER 8-3: INTCON3 REGISTER

R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF
bit 7							bit 0

bit 7 **INT2IP:** INT2 External Interrupt Priority bit
1 = High priority
0 = Low priority

bit 6 **INT1IP:** INT1 External Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5 **Unimplemented:** Read as '0'

bit 4 **INT2IE:** INT2 External Interrupt Enable bit
1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt

bit 3 **INT1IE:** INT1 External Interrupt Enable bit
1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt

bit 2 **Unimplemented:** Read as '0'

bit 1 **INT2IF:** INT2 External Interrupt Flag bit
1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur

bit 0 **INT1IF:** INT1 External Interrupt Flag bit
1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur

INTCON3 = 0b00001000;

Interrupt Registers (2)

REGISTER 8-10: RCON REGISTER

R/W-0	U-0	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (16CXXX Compatibility mode)

bit 6-5 **Unimplemented:** Read as '0'

bit 4 $\overline{RI}$: RESET Instruction Flag bit
For details of bit operation, see Register 4-3

bit 3 $\overline{TO}$: Watchdog Time-out Flag bit
For details of bit operation, see Register 4-3

bit 2 $\overline{PD}$: Power-down Detection Flag bit
For details of bit operation, see Register 4-3

bit 1 $\overline{POR}$: Power-on Reset Status bit
For details of bit operation, see Register 4-3

bit 0 $\overline{BOR}$: Brown-out Reset Status bit
For details of bit operation, see Register 4-3

RCON =0x80

Παράδειγμα χρήσης INTERRUPT (1)

```
void interrupt() {
      PORTC.F0 =1;   //arm relay1
      INTCON =  0b11010000;  //καθαρισμός  interrupt flag
}

 void interrupt_low() {
      PORTC.F0 =0;    //disarm relay1
      INTCON3 = 0b00001000;  //καθαρισμός  interrupt flag
}
```

Παράδειγμα χρήσης INTERRUPT (2)

```
void main()
{
   unsigned char i= 0x30;

   TRISC = 0x00;

   INTCON =  0b11010000;
   INTCON3 = 0b00001000;
   RCON =0x80;

   Lcd8_Config(&PORTE, &PORTD, 2,1,0, 7,6,5,4,3,2,1,0);
   Lcd8_Cmd(LCD_CURSOR_OFF); // Turn off blinking cursor
   Lcd8_Cmd(LCD_CLEAR);      // Clear screen

   Lcd8_Out(1, 1, "INTERRUPT"); // Print text on LCD
   while (1){
       Lcd8_Chr(2,5, i);
       i++;
       if (i>0x7A) i=0x20;
  }
}
```

Κώδικας Interrupt Service Routine

```
$0000   $EF47   F001                        GOTO    _main
$0008   $EF2C   F000                        GOTO    _interrupt
$0058   $       _interrupt:
$0058   $CFE9   F01A                        MOVFF   FSR0L, ?saveFSR0
$005C   $CFEA   F01B                        MOVFF   FSR0H, ?saveFSR0+1
$0060   $CFE1   F01C                        MOVFF   FSR1L, ?saveFSR1
$0064   $CFE2   F01D                        MOVFF   FSR1H, ?saveFSR1+1
;INTERRUPT_DEMO.c,1 ::      void interrupt() {
;INTERRUPT_DEMO.c,2 ::      PORTC.F0 =1;   //arm relay1
$0068   $8082                               BSF     PORTC, 0, 0
;INTERRUPT_DEMO.c,3 ::                      INTCON = 0b11010000;
$006A   $0ED0                               MOVLW   208
$006C   $6EF2                               MOVWF   INTCON, 0
;INTERRUPT_DEMO.c,4 ::      }//~
$006E   $       L_Interrupt_end:
$006E   $C01A   FFE9                        MOVFF   ?saveFSR0, FSR0L
$0072   $C01B   FFEA                        MOVFF   ?saveFSR0+1, FSR0H
$0076   $C01C   FFE1                        MOVFF   ?saveFSR1, FSR1L
$007A   $C01D   FFE2                        MOVFF   ?saveFSR1+1, FSR1H
$007E   $0011                               RETFIE
```

Κώδικας Interrupt Service Routine

```
$0018    $           _interrupt_low:
$0018    $CFE8       F01E                    MOVFF    WREG, ?Low_saveWERG
$001C    $CFD8       F01F                    MOVFF    STATUS, ?Low_saveSTATUS
$0020    $CFE0       F020                    MOVFF    BSR, ?Low_saveBSR
$0024    $CFE9       F01A                    MOVFF    FSR0L, ?saveFSR0
$0028    $CFEA       F01B                    MOVFF    FSR0H, ?saveFSR0+1
$002C    $CFE1       F01C                    MOVFF    FSR1L, ?saveFSR1
$0030    $CFE2       F01D                    MOVFF    FSR1H, ?saveFSR1+1
;INTERRUPT_DEMO.c,6 ::          void interrupt_low() {
;INTERRUPT_DEMO.c,7 ::          PORTC.F0 =0;    //disarm relay1
$0034    $9082                               BCF      PORTC, 0, 0
;INTERRUPT_DEMO.c,8 ::          INTCON3 = 0b00001000;
$0036    $0E08                               MOVLW    8
$0038    $6EF0                               MOVWF    INTCON3, 0
;INTERRUPT_DEMO.c,9 ::          }
$003A    $           L_Low_Interrupt_end:
$003A    $C01E       FFE8                    MOVFF    ?Low_saveWERG, WREG
$003E    $C01F       FFD8                    MOVFF    ?Low_saveSTATUS, STATUS
$0042    $C020       FFE0                    MOVFF    ?Low_saveBSR, BSR
$0046    $C01A       FFE9                    MOVFF    ?saveFSR0, FSR0L
$004A    $C01B       FFEA                    MOVFF    ?saveFSR0+1, FSR0H
$004E    $C01C       FFE1                    MOVFF    ?saveFSR1, FSR1L
$0052    $C01D       FFE2                    MOVFF    ?saveFSR1+1, FSR1H
$0056    $0010                               RETFIE   0
```